CCD5061
6K x 128 Element
TDI – Time, Delay and Integration

FEATURES

- **6144 pixels per line**
- **Number of TDI stages electronically selectable: 4, 8, 16, 32, 64, 96, 128**
- **Bi-directional TDI (shift up or down)**
- **8 outputs—each capable of 20MHz data rate—80 MHz total data rate per side (shift up or down)**
- **100% fill factor**
- **8.75µm x 8.75µm pixel size**
- **On-chip binning capability**

GENERAL DESCRIPTION

The CCD5061 is a 6144 pixel x 128 line, high speed TDI sensor. The active imaging area is organized as 6144 vertical columns and 128 horizontal TDI rows. The array is set up for bi-directional operation. There are identical output registers and amplifiers on both the top and the bottom of the array. The outputs to be used (either top or bottom) are user-selectable and controlled by the vertical clock timing. In addition, the exposure level can be controlled by reducing the number of TDI rows from 128 to 96, 64, 32, 16, 8 or 4. This is also user-selectable and is accomplished by supplying the appropriate phasing for the vertical clocks within each section. For instance, if 64 lines of TDI were required, the vertical clocks for lines 65-128 would be connected to a high potential, which would drain these unused rows out to the opposite side (unused) of the array to be dumped into the VOFD drain. With four outputs, each running at 20MHz, the CCD5061 can provide a total data rate of 80MHz enabling the CCD to run at better than 12kHz line rate. Utilizing Fairchild Imaging proprietary buried channel CCD process, the CCD5061 achieves consistent, superior TDI performance.

The active imaging area is separated from the four horizontal output registers by 21 isolation rows. These isolation rows are covered by a metal lightshield to protect them while charge transfers to the output registers. Both the active imaging area and the isolation region utilize 3-phase clocking.

The four horizontal output registers utilize 4-phase clocking. Special design techniques have been implemented to maximize charge transfer efficiency especially at low light levels. The output amplifier is a 3-stage source follower configuration. This allows maximum scale factor (charge to voltage conversion) and maximum bandwidth.

The CCD5061 is housed in a custom 176 pin (100 mil grid) ceramic PGA package. It has an AR coated window.

FUNCTIONAL DESCRIPTION

The following functional elements are illustrated in the block diagram:

Image Sensing Elements: These are elements of a line of 6144 image sensors separated by channel stops and covered by a passivation layer. Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photoelectrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear

function of the localized incident illumination intensity and integration period.

Transfer Gates: This gate is a structure adjacent to the row of image sensor elements. The charge packets accumulated in the photosites are transferred in parallel via the transfer gate to the transport shift registers whenever the transfer gate voltage goes high.

Shift Registers: The vertical shift register is 3-phase and the horizontal shift register is 4-phase.

Time Delay and Integration: This function is accomplished by scanning the image scene across the array at the same rate as the vertical shift register moves the signal charge. This results in an effective increase in the integration time.

Output Amplifier: The CCD5061 is designed for either uni-directional or bi-directional operation. There are four identical output registers and amplifiers on both the top and bottom of the array. There are three-stage source follower amplifiers with a reset MOSFET tied to the input gate.

Charge packets are clocked to a pre-charged capacitor whose potential changes linearly in response to the number of electrons delivered. This potential is applied to the input gate of an NMOS amplifier producing a signal at the output V_{out} pin. The capacitor is reset with ϕR to a pre-charge level prior to the arrival of the next charge packet except when horizontally binning. It is reset by use of the reset MOSFET.

The output amplifier drain is tied to VDD. The source is connected to an external load resistor to ground. The source constitutes the video output from the device.

DEFINITION OF TERMS

Charge-Coupled Device: A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Isolation Rows: There are 21 isolation rows between the image area and the horizontal shift register. These non-imaging rows are used as buffer rows to eliminate crosstalk to the horizontal shift register.

Dynamic Range: The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

RMS Noise Equivalent Exposure: The exposure level that gives an output signal equal to the RMS noise level at the output in the dark.

Saturation Exposure: The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Charge Transfer Efficiency: Percentage of valid charge information that is transferred between each successive stage of the transport register.

Responsivity: The output signal voltage per unit of exposure.

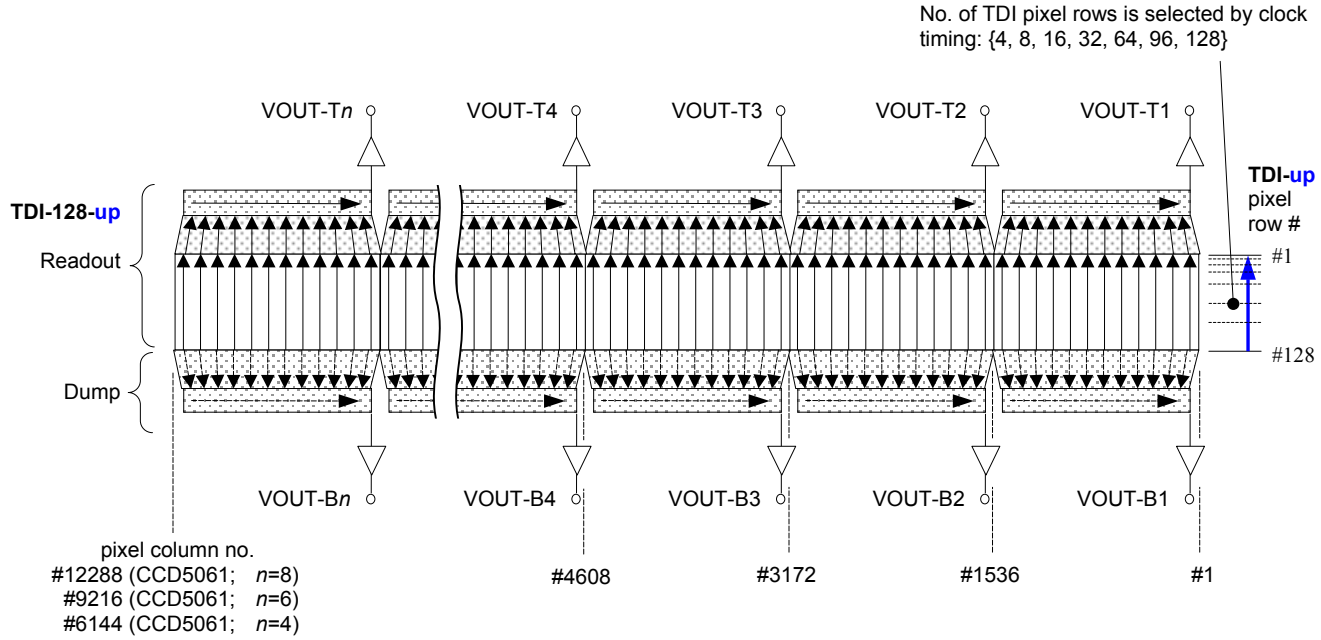
Photo-Response Non-Uniformity: The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

Dark Signal: The output signal caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

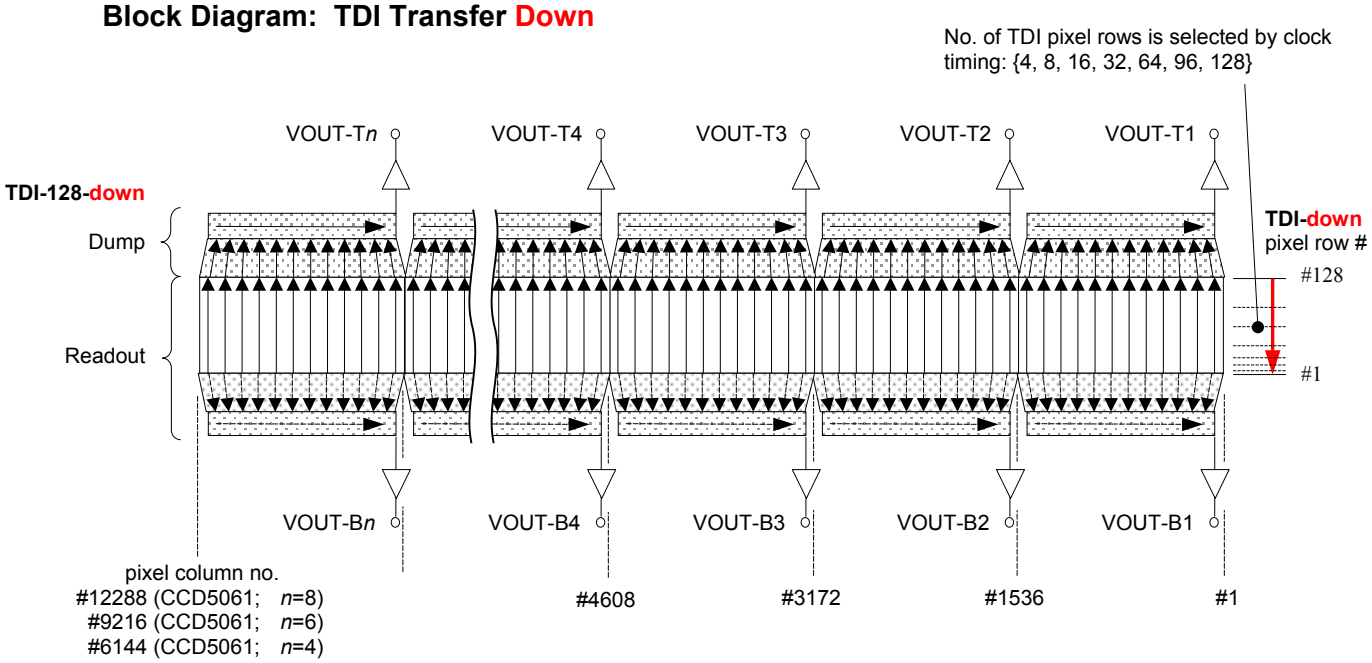
Integration Time: The time interval between the falling edges of any two successive transfer pulses is the integration time shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel: Picture element or sensor element, also called photoelement or photosite.

Block Diagram: TDI Transfer Up

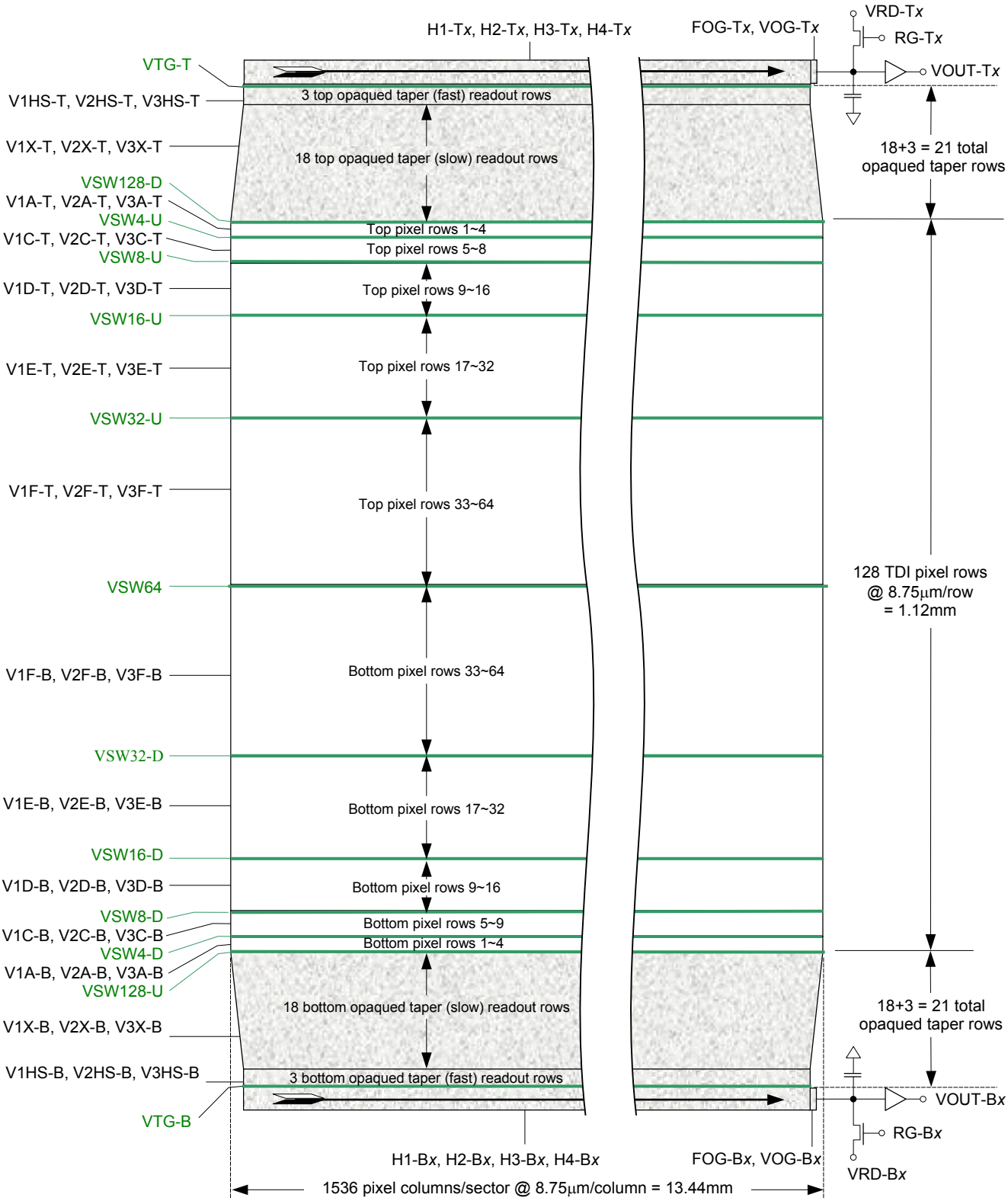


Block Diagram: TDI Transfer Down



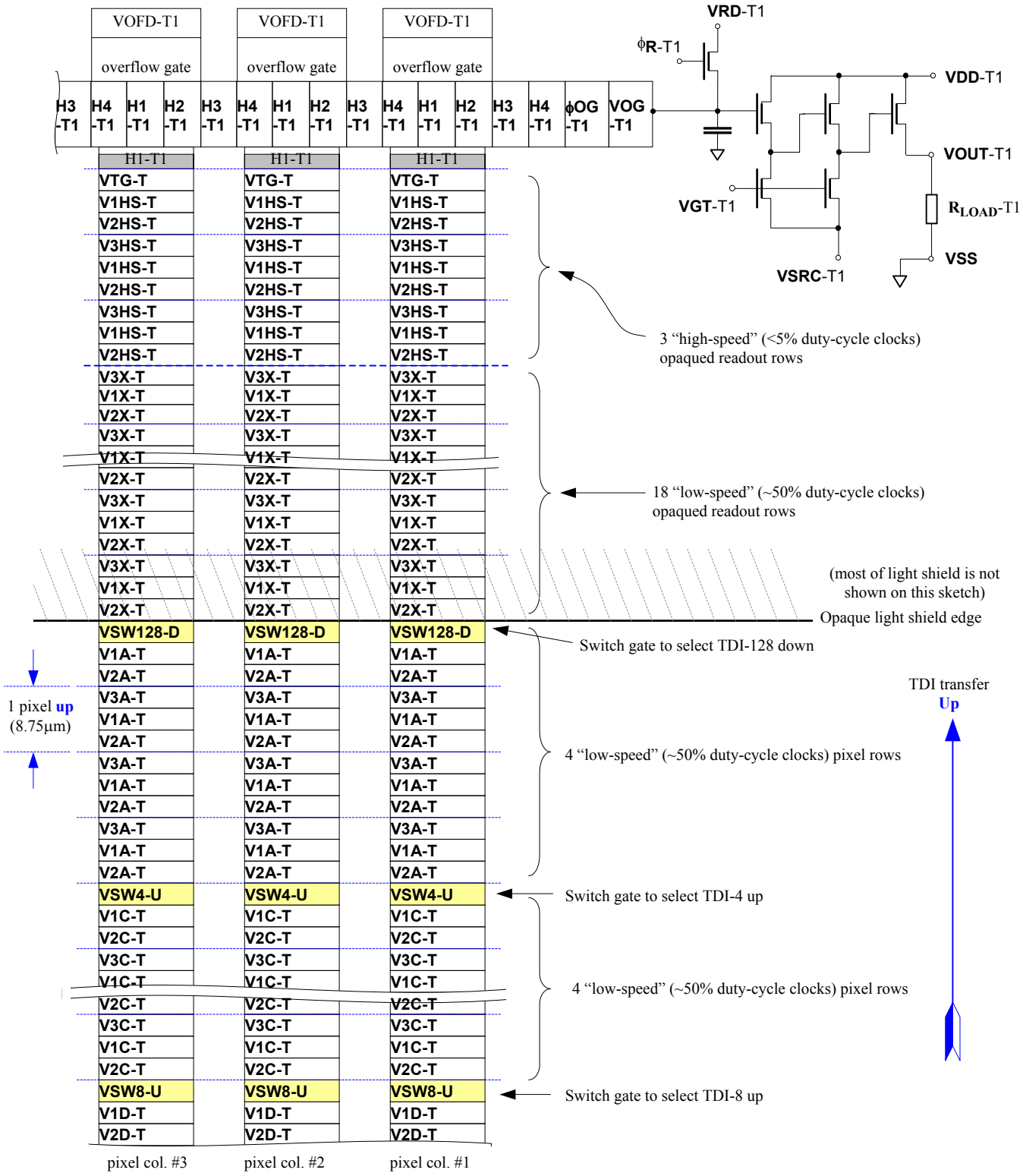
Block Diagram of Sector "*x*"

(where *x*={1, 2, …8} for CCD5061, *x*={1, 2, ...6} for CCD5061, *x*={1, 2, …4} for CCD5061.)

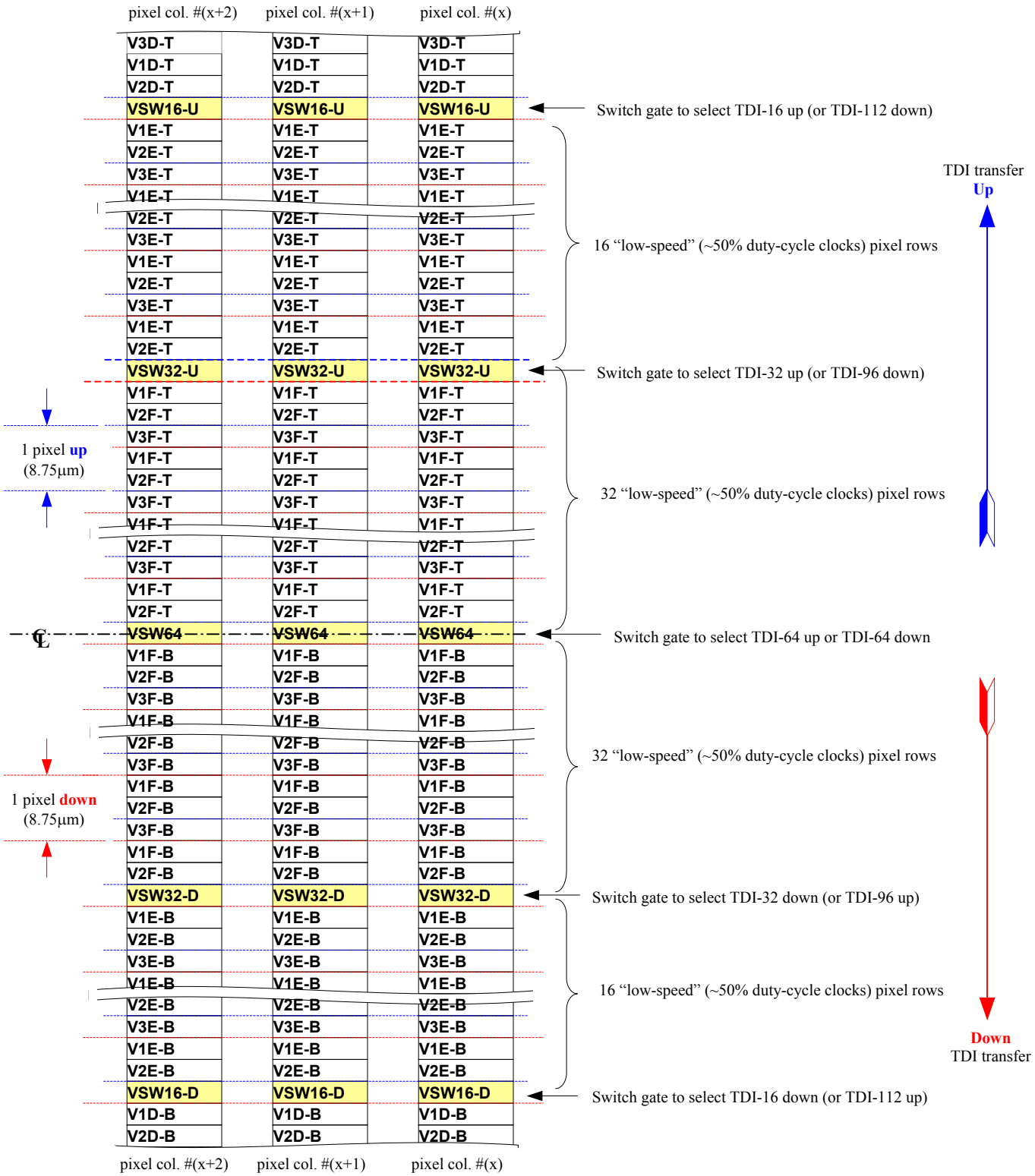


Block Diagram at Sector T1 Output Amplifier

(All top sectors T1, T2, …T8 have this design.)

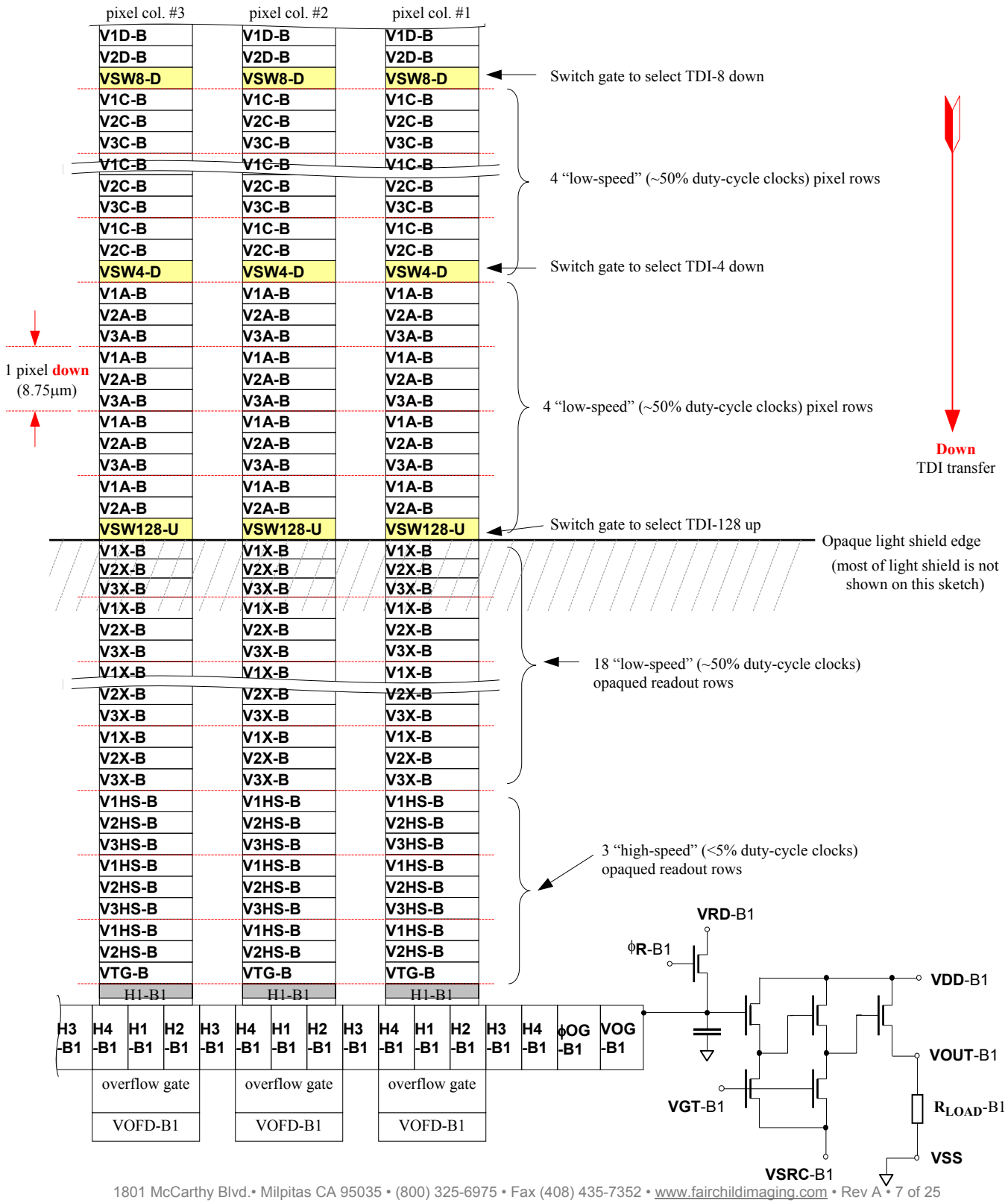


Block Diagram at Pixel Array Vertical Centerline



Block Diagram at Sector B1 Output Amplifier

(All bottom sectors B1, B2,…B8 have this design.)

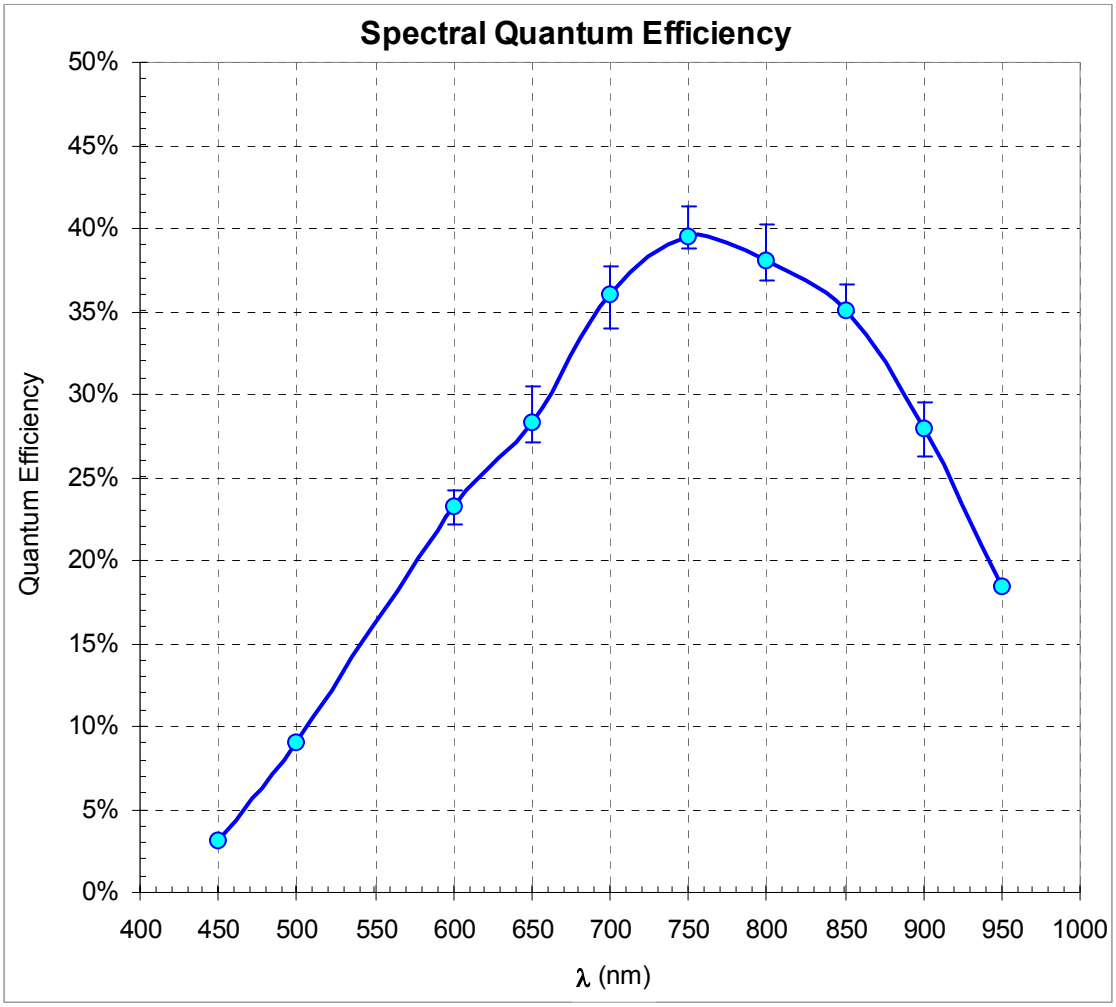


CCD5061 Device Architecture	
Pixel array (across-the-TDI-scan)	6144 pixels per line = 4 sectors x 1,536 pixels/sector
Pixel array (along-the-TDI-scan)	Clock-selectable: {4, 8, 16, 32, 64, 96, or 128} pixels / TDI column
TDI transfer direction	Bi-directional (“up” or “down”)
Pixel size	8.75µm x 8.75µm
Image format	53.76 mm x 1.12mm
Number of output ports	4 @ Top (transfer “up”), 4 @ Bottom (transfer “down”)
Pixel rate / output (max)	20M pixel/s / output
Total pixel output rate (max)	80M pixel/s = 20M pixel/s/output x 4 outputs
Vertical (“parallel”) shift registers	3-phase
Number of isolation rows	21 top, 21 bottom (all covered by opaque light shield)
Horizontal (“serial”) shift registers	4-phase

CCD5061 Performance Specifications					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units / Remarks**
H-Q_{SAT}	Horizontal Saturation Charge (“Full Well”)	500	550		ke- at 12k lines/s
V-Q_{SAT}	Vertical Saturation Charge (“Full Well”)	450	500		ke- at 12k lines/s
CG	Conversion Gain	2.5	3.3	4.0	µV/e-
V_{SAT}	Saturation Voltage		1.5		V
VLIN	Non-Linearity		1%	5%	@ 10% to 90% Full Well
DR	Dynamic Range		10,000		DR = Q_{SAT} / NE
H-CTE	Horizontal CTE	0.999985	0.999995		/transfer (4 H-transfers/pixel)
V-CTE	Vertical CTE	0.99980	0.99995		/transfer (3 V-transfers/pixel)
NE	Read Noise		40	50	e-rms
PRNU	Photoresponse Non-Uniformity		5	20	% pk-pk
F_{PIXEL}	Pixel Array Flatness		30		µm pk-pk (note 1)
DS	Dark Signal		1.3	6	nA/cm^2 at +25°C
-----	DC offset on VOUT pins		15		V
P_{AMPS}	Power dissipation: output amps		0.9		W (note 2)
$P_{H\text{-}CLK}$	Power dissipation: H-clocks		1.4		W (note 3)
$P_{V\text{-}CLK}$	Power dissipation: V-clocks		0.1		W (note 3)

Note 1: Measured to the best-fit plane to the pixel array. F_{PIXEL}<13µm pk-pk is available on special order.
Note 2: Power dissipated in R_{LOAD} resistors (which are not inside the CCD package) is not included in this total.
Note 3: Clock power dissipation is proportional to $C*V^2*f$

TEST CONDITIONS: All testing performed at:
- Temp = +25ºC typ.
- Horizontal clock frequency = 20MHz / output & Vertical clock frequency = 12kHz
- Input voltages and load resistors R_{LOAD} at typical values, except (a) horizontal register clock offsets may be tuned as required to optimize performance, and (b) {H1, H2, H3, & H4} clock swings ≤6Vpp.
- Q_{SAT} and V_{SAT} measured in TDI-128-up and TDI-128-down modes. FF (Full-frame) mode may be used as convenient to measure other parameters.
- No binning: 1x1 full-resolution mode.



Typical QE Curve for CCD5061

Output Amplifier Voltages & External Load Resistor						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
VDD	Amplifier DC Supply		+23		V	$I_{DD} \cong$+15mA /pin. See note 1
VRD	Reset Drain		+16		V	See note 1
VOFD	Overflow Drain		+16		V	See note 2
VSRC	Current source (“signal ground”) from amplifier 1st & 2nd stages		+2.5		V	$I_{SRC} \cong$ -1.5mA /pin
VGT	Bias voltage for amplifier 1st & 2nd-stage constant-current-source FETs		+4		V	I_{GT} < 1nA /pin
VOG	Output Gate DC Bias		-4		V	I_{OG} < 1nA /pin
VSS	Substrate [Ground]		0		V	
R_{LOAD}	Output Load on each VOUT pin to VSS	0.9	1.0		kΩ	If the external preamp has <100kΩ equivalent input resistance, then increase R_{LOAD} so that the total equivalent resistance from VOUT to VSS is 1.0kΩ

Note 1: Whenever VDD>+12V, VRD must be biased at not less than 12V less than VDD:

$VRD \geq (VDD-12V)$, for all VDD>+12V

A zener diode circuit is recommended to ensure that this condition is always met. If this condition is not met, even momentarily, then permanent damage to the output amplifier(s) may result.

Note 2: (VRD-2V)<VOFD<(VRD+2V) If this condition is not met, even momentarily (for example, during power-up or power-down), then permanent damage to the CCD gates may result.

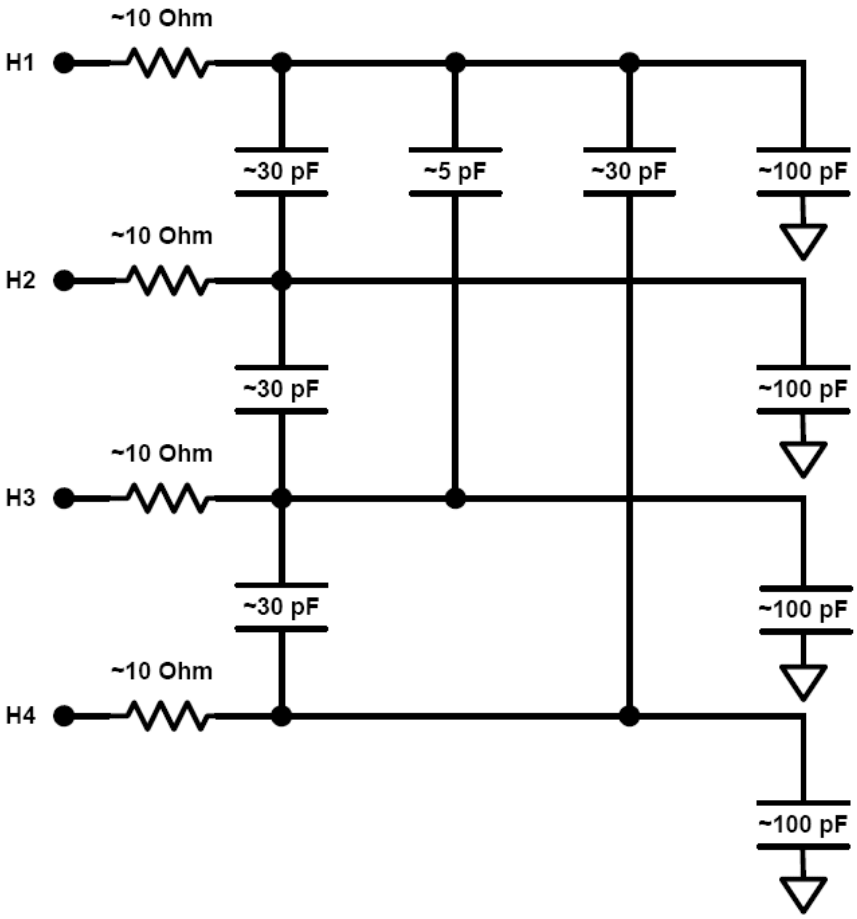
Absolute Maximum Ratings				
Pin Names (suffixes not listed below)	**Min**	**Max**	**Unit**	**Remarks**
VSS	0	0	V	Must be grounded to 0V when device is being handled. Do not “float”.
VDD, VRD, VOFD, VOUT, VSRC, VGT	-0.4	+25	V	Each pin has a diode to VSS on the chip
All other pins	-5	+20	V	
Δ Voltage between adjacent CCD gates	-24	+24	V	Block diagram shows adjacent gates.
Storage temperature	-40	+70	°C	
Operating temperature	-40	+60	°C	

Clock Voltages						
Name	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
V1, V2	"Slow" (~50% duty cycle) vertical shift register clocks					
	Clock-High		+18		V	Readout side
	Clock-Low		0		V	Readout side
	V-dump		+15		V	Dump side
V3	"Slow" (~50% duty cycle) vertical shift register clock					
	Clock-High		+18		V	Readout side
	Clock-Low		0		V	Readout side
	V-dump		+15		V	Dump side
	V-off		-3		V	For VSWxx TDI-length-control gate at the selected readout/dump boundary
V1-HS, V2-HS, V3-HS	"Fast" (<5% duty cycle) vertical shift register clocks (3 isolation rows nearest Horizontal shift registers)					
	Clock-High		+15		V	Readout side
	Clock-Low		0		V	Readout side
	V-dump		+15		V	Dump side
H1, H2, H3, H4	Horizontal shift register clocks					
	Clock-High		4		V	Note 1
	Clock-Low		-1		V	Note 1
	H-dump		+4		V	Dump side
ϕOG (FOG)	Clocked output gate					
	Clock-High		+1		V	Note 1
	Clock-Low		-5		V	Note 1
	H-dump		+3		V	Dump side (or set to ϕOG clock-high)
ϕR (RG)	Reset gate clock					
	Clock-High		+15		V	
	Clock-Low		+4		V	
	H-dump		+3		V	Dump side (or set to ϕR clock-high)

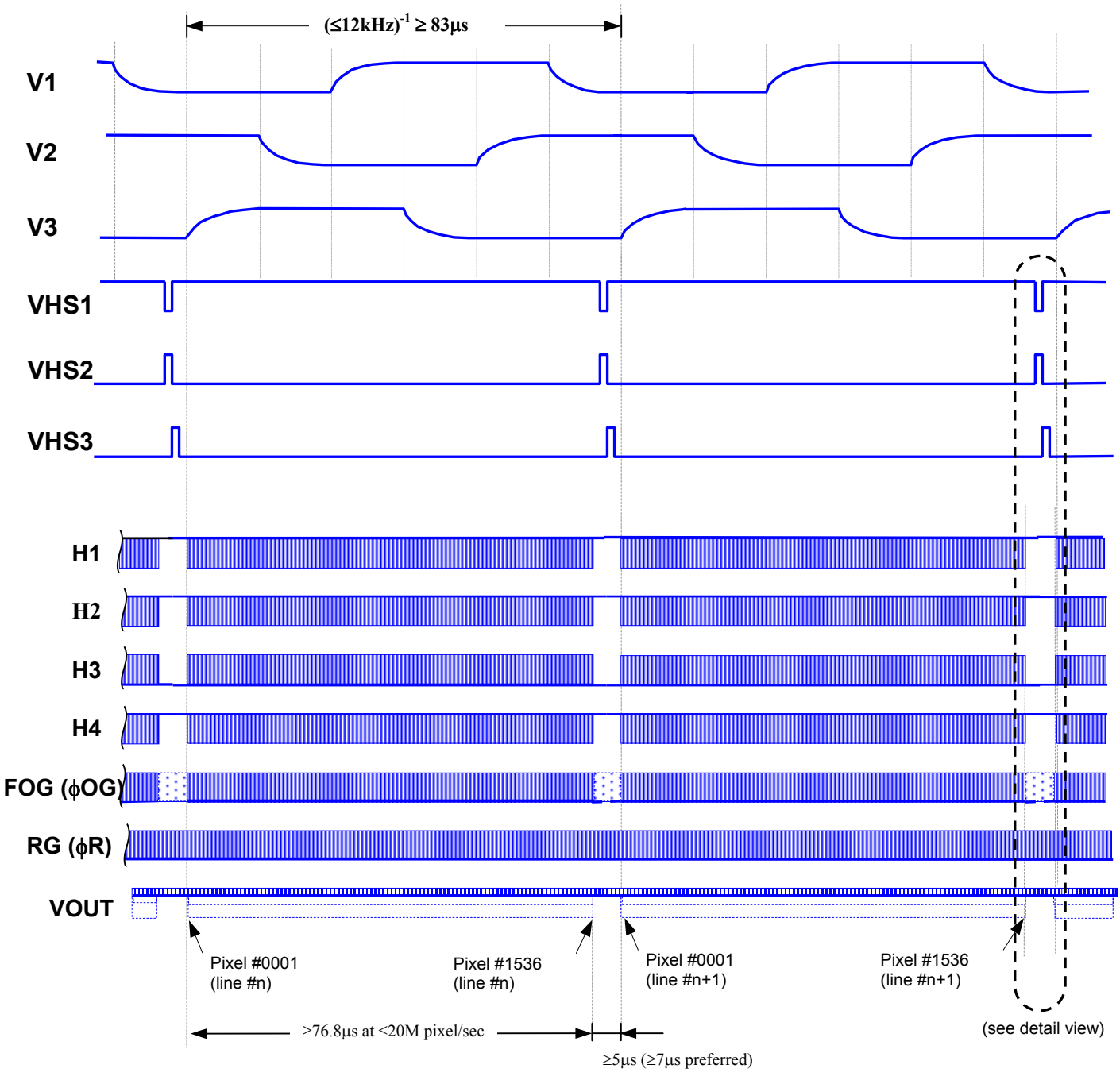
Note 1: May require individually tuned voltages for optimum performance, especially at high speed.

CCD5061 Clock Capacitance				
Symbol	**Parameter**	**Typ**	**Unit**	**Remarks**
Photosite rows: V1, V2, V3: capacitance per pixel row				
	V1 to VSS	8	pF	
	V1 to V2	10	pF	
	V1 to V3	9	pF	
	V2 to VSS	12	pF	
	V2 to V3	11	pF	
	V3 to VSS	11	pF	
Isolation and high-speed rows: capacitance per row				
	V1 to VSS	10	pF	
	V1 to V2	10	pF	
	V1 to V3	9	pF	
	V2 to VSS	15	pF	
	V2 to V1 (see above)			
	V2 to V3	11	pF	
	V3 to VSS	16	pF	
	V3 to V1 (see above)			
	V3 to V2 (see above)			
Horizontal transport gate and reset gate capacitance per 1536-element output section				
	H1, H2, H3, H4	165	pF	
	ΦOG	10	pF	
	ΦR	10	pF	

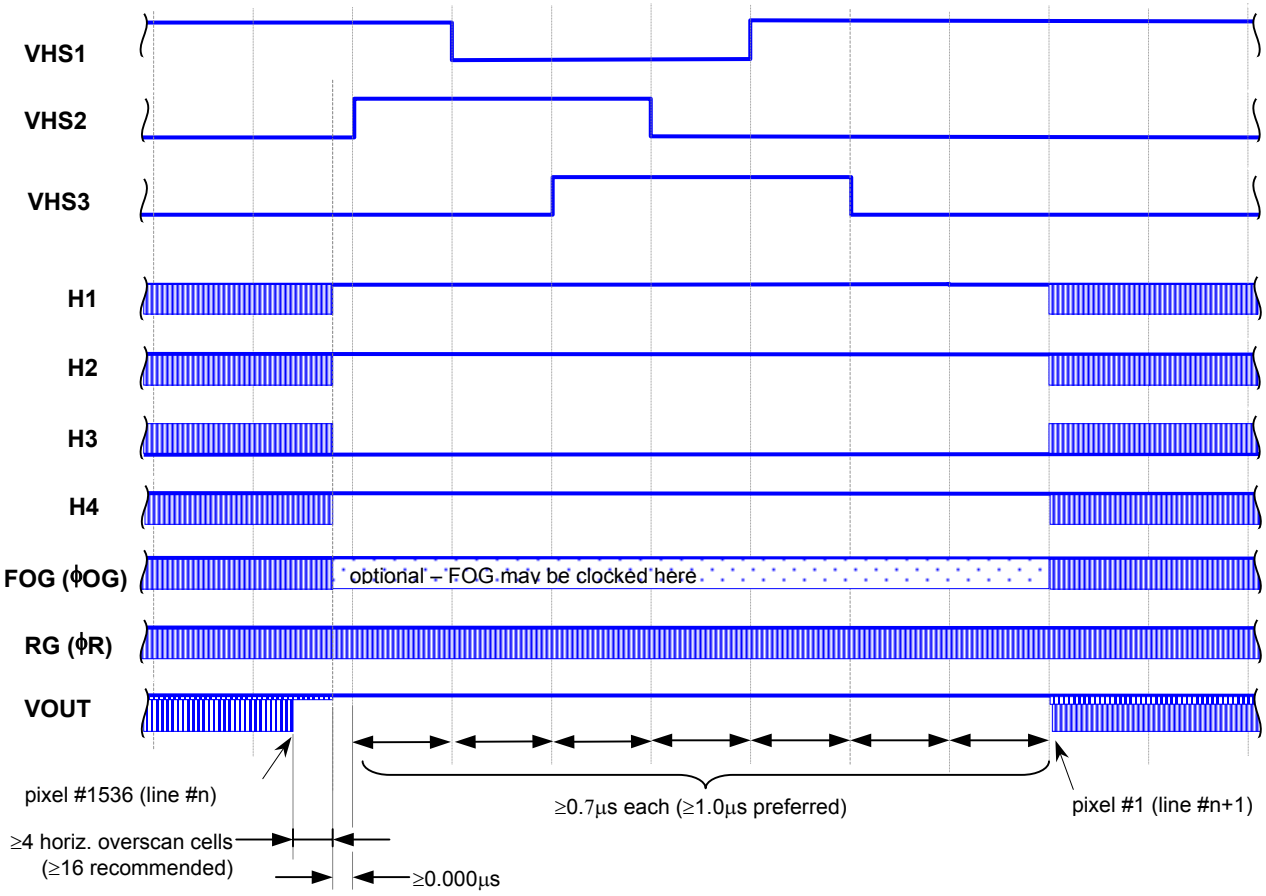
Horizontal Clock Capacitance Network



Clock Timing Overview (1x1 full-resolution mode)



Vertical-to-Horizontal Clock Timing (1x1 full-resolution mode)

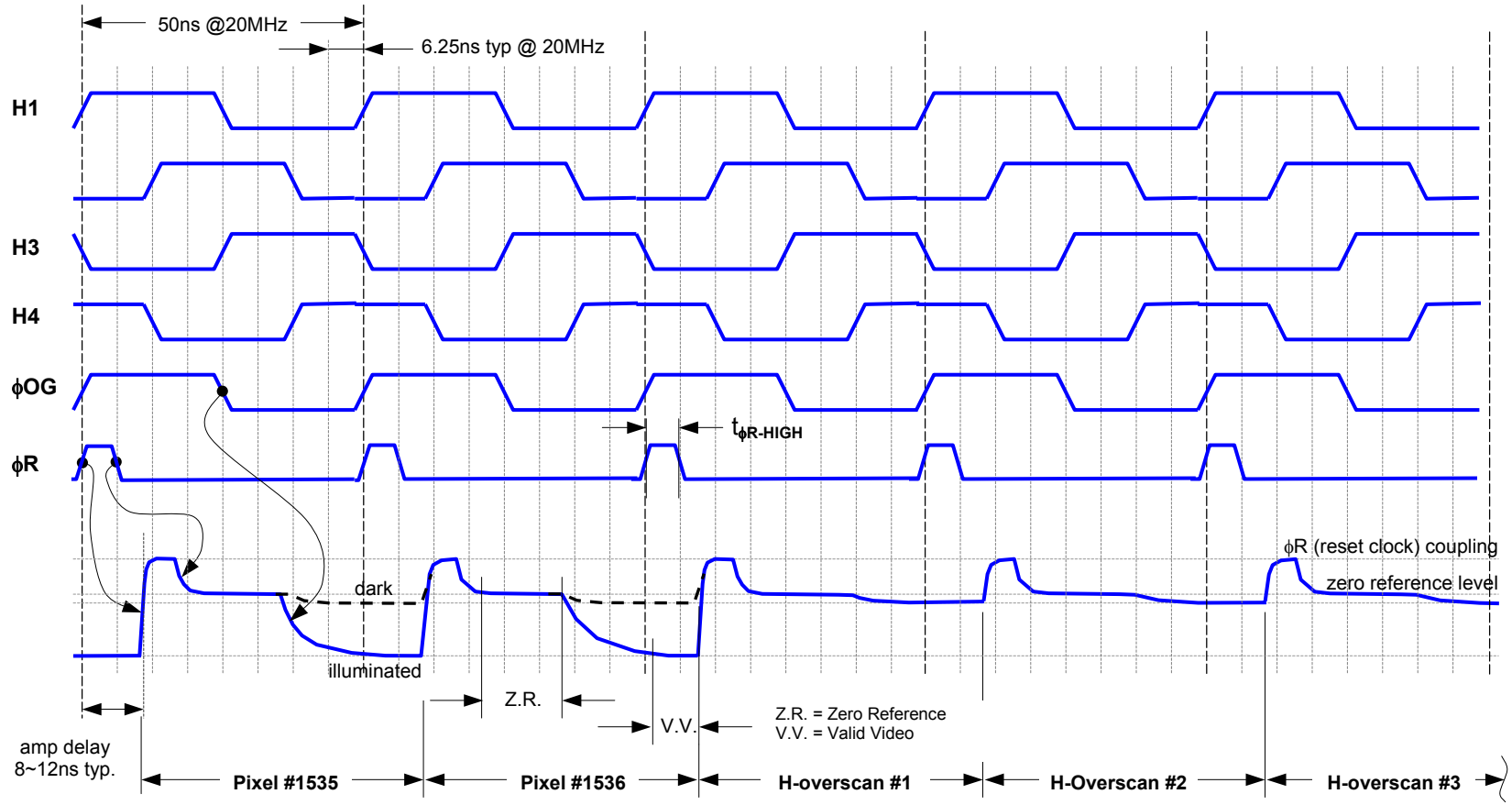


Clock Timing (parameters not otherwise specified on timing diagrams)

Clock	Parameter(s)	Typ	unit	Notes
V1, V2	t_{RISE}(0%→90%), t_{FALL}(100%→10%)	4	µs	(1)
V3	t_{RISE}(0%→90%), t_{FALL}(100%→10%)	7	µs	(1)
VHS1, VHS2, VH3	t_{RISE}(0%→90%), t_{FALL}(100%→10%)	0.3	µs	
H1, H2, H3, H4	t_{RISE}(0%→90%), t_{FALL}(100%→10%)	2	ns	
H1	$t_{TRILEVEL}$	0.3	µs	
ϕOG (FOG)	t_{RISE}(0%→90%), t_{FALL}(100%→10%)	2	ns	
ϕR (RG)	t_{RISE}(0%→90%), t_{FALL}(100%→10%)	1	ns	
ϕR (RG)	$t_{\phi R\text{-}HIGH}$	4	ns	

(1) Use typical values to maximize QSAT at LineRate=12,000 pixel_lines/s.

4-phase Horizontal Clock Timing (1x1 full-resolution mode)



For best results, especially at high speed (20MHz), use:

- {H1, H2, H3, H4, ϕOG} duty cycle = 50%
- H1 falling edge is at same time as H3 rising edge, H1 rising edge is same time as H3 falling edge → H1 clock glitches cancel H3 clock glitches.
- H2 falling edge is at same time as H4 rising edge, H2 rising edge is same time as H4 falling edge → H2 clock glitches cancel H4 clock glitches.
- H1 and ϕOG have identical clock timing (although H1 clock voltage may not be same as ϕOG clock voltage).

Pin Name and Description		
Pin Name	**Signal Description**	**Remarks**
VTG-T	Vertical-to-horizontal transfer gate – top	
V1HS-T, V2HS-T, V3HS-T	Fast (<5% duty cycle) vertical shift register gates – top 3 opaqued rows	
V1X-T, V2X-T, V3X-T	Slow (~50% duty cycle) vertical shift register gates – next 18 opaqued top rows	(1)
VSW128-D	Slow (~50% duty cycle) vertical shift register V3 gate – top pixel row #1	(1), Connect to V-OFF for TDI-128-down
V1A-T, V2A-T, V3A-T	Slow (~50% duty cycle) vertical shift register gates – top pixel rows #1~#4	(1)
VSW4-U	Slow (~50% duty cycle) vertical shift register V3 gate – top pixel row #4	(1), Connect to V-OFF for TDI-4-up
V1C-T, V2C-T, V3C-T	Slow (~50% duty cycle) vertical shift register gates – top pixel rows #5~#8	(1)
VSW8-U	Slow (~50% duty cycle) vertical shift register V3 gate – top pixel row #8	(1), Connect to V-OFF for TDI-8-up
V1D-T, V2D-T, V3D-T	Slow (~50% duty cycle) vertical shift register gates – top pixel rows #9~#16	(1)
VSW16-U	Slow (~50% duty cycle) vertical shift register V3 gate – top pixel row #16	(1), Connect to V-OFF for TDI-16-up
V1E-T, V2E-T, V3E-T	Slow (~50% duty cycle) vertical shift register gates – top pixel rows #17~#32	(1)
VSW32-U	Slow (~50% duty cycle) vertical shift register V3 gate – top pixel row #32	(1), Connect to V-OFF for TDI-32-up, Connect to V-OFF for TDI-96-down
V1F-T, V2F-T, V3F-T	Slow (~50% duty cycle) vertical shift register gates – top pixel rows #33~#64	(1)
VSW64-U	Slow (~50% duty cycle) vertical shift register V3 gate – top pixel row #64	(1), Connect to V-OFF for TDI-64-up, Connect to V-OFF for TDI-64-down
V1F-B, V2F-B, V3F-B	Slow (~50% duty cycle) vertical shift register gates – bottom pixel rows #33~#64	(1)
VSW32-D	Slow (~50% duty cycle) vertical shift register V3 gate – bottom pixel row #32	(1) Connect to V-OFF for TDI-32-down, Connect to V-OFF for TDI-96-up
V1E-B, V2E-B, V3E-B	Slow (~50% duty cycle) vertical shift register gates – bottom pixel rows #17~#32	(1)
VSW16-D	Slow (~50% duty cycle) vertical shift register V3 gate – bottom pixel row #16	(1), Connect to V-OFF for TDI-16- down
V1D-B, V2D-B, V3D-B	Slow (~50% duty cycle) vertical shift register gates – bottom pixel rows #9~#16	(1)
VSW8-D	Slow (~50% duty cycle) vertical shift register V3 gate – bottom pixel row #8	(1), Connect to V-OFF for TDI-8- down
V1C-B, V2C-B, V3C-B	Slow (~50% duty cycle) vertical shift register gates – bottom pixel rows #5~#8	(1)
VSW4-D	Slow (~50% duty cycle) vertical shift register V3 gate – bottom pixel row #4	(1), Connect to V-OFF for TDI-4- down
V1A-B, V2A-B, V3A-B	Slow (~50% duty cycle) vertical shift register gates – bottom pixel rows #1~#4	(1)
VSW128-U	Slow (~50% duty cycle) vertical shift register V3 gate – bottom pixel row #1	(1), Connect to V-OFF for TDI-128-up
V1X-B, V2X-B, V3X-B	Slow (~50% duty cycle) vertical shift register gates – next 18 opaqued bottom rows	(1)
V1HS-B, V2HS-B, V3HS-B	Fast (<5% duty cycle) vertical shift register gates – bottom 3 opaqued rows	

Pin Name and Description		
Pin Name	**Signal Description**	**Remarks**
VTG-B	Vertical-to-horizontal transfer gate – bottom	
H1-Tx, H2-Tx, H3-Tx, H4-Tx	4-phase horizontal shift register gates, top sector Tx	(2)
H1-Bx, H2-Bx, H3-Bx, H4-Bx	4-phase horizontal shift register gates, bottom sector Bx	(2)
FOG-yx (ϕOG-yx)	Horizontal shift register summing gate, sector yx	(2), (3)
RG-yx (ϕR-yx)	Reset gate, sector yx	(2), (3)
VDD-yx	Amplifier power supply, sector yx	(2), (3)
VRD-yx	Reset drain, sector yx	(2), (3)
VOFD-yx	Overflow drain, sector yx	(2), (3)
VSRC-yx	Amplifier1st-stage and 2nd-stage load source (sinks ~1.25mA / pin), sector yx	(2), (3)
VGT-yx	Amplifier 1st-stage and 2nd-stage load current control (gate bias), sector yx	(2), (3)
VSS	Substrate (ground)	Connect all VSS pins to 0V
TEMP-yx	*(optional; not installed on standard devices)* 100kΩ thermistor temp sensor	

(1) All slow vertical shift register gates have identically-named pins at both ends of the CCD package. For each of these gates, connect both ends to the clock driver. Do not drive from one end only; this will reduce QSAT at high line rates.

(2) x = sector number: CCD5061: x={1, 2, 3, …8}; CCD5061: x={1, 2, 3, …6}; CCD5061: x={1, 2, 3, 4}.

(3) y = TDI transfer direction: y={T, B} for Top (transfer up) or Bottom (transfer down).

Pin Connection Table for each TDI mode

Pin Name	TDI-4 UP	TDI-8 UP	TDI-16 UP	TDI-32 UP	TDI-64 UP	TDI-96 UP	TDI-128 UP	TDI-4 DOWN	TDI-8 DOWN	TDI-16 DOWN	TDI-32 DOWN	TDI-64 DOWN	TDI-96 DOWN	TDI-128 DOWN
VDD-Tx	VDD	VDD	VDD	VDD	VDD	VDD	VDD	(note 4)	(note 4)	(note 4)	(note 4)	(note 4)	(note 4)	(note 4)
VSRC-Tx	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC
VGT-Tx	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT
VRD-Tx	VRD	VRD	VRD	VRD	VRD	VRD	VRD	VRD	VRD	VRD	VRD	VRD	VRD	VRD
VOFD-Tx	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD
RG-Tx	ϕR	ϕR	ϕR	ϕR	ϕR	ϕR	ϕR	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)
FOG-Tx	ϕOG	ϕOG	ϕOG	ϕOG	ϕOG	ϕOG	ϕOG	(note 2)	(note 2)	(note 2)	(note 2)	(note 2)	(note 2)	(note 2)
H1-Tx	H1	H1	H1	H1	H1	H1	H1	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump
H2-Tx	H2	H2	H2	H2	H2	H2	H2	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump
H3-Tx	H3	H3	H3	H3	H3	H3	H3	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump
H4-Tx	H4	H4	H4	H4	H4	H4	H4	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump
VTG-T	VHS3	VHS3	VHS3	VHS3	VHS3	VHS3	VHS3	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump
V1HS-T	VHS2	VHS2	VHS2	VHS2	VHS2	VHS2	VHS2	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump
V2HS-T	VHS1	VHS1	VHS1	VHS1	VHS1	VHS1	VHS1	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump
V3HS-T	VHS3	VHS3	VHS3	VHS3	VHS3	VHS3	VHS3	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump
V1X-T	V2	V2	V2	V2	V2	V2	V2	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump
V2X-T	V1	V1	V1	V1	V1	V1	V1	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump
V3X-T	V3	V3	V3	V3	V3	V3	V3	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump
VSW128-D	V3	V3	V3	V3	V3	V3	V3	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-OFF
V1A-T	V2	V2	V2	V2	V2	V2	V2	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V1
V2A-T	V1	V1	V1	V1	V1	V1	V1	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V2
V3A-T	V3	V3	V3	V3	V3	V3	V3	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3
VSW4-U	V-OFF	V3	V3	V3	V3	V3	V3	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3
V1C-T	V-dump	V2	V2	V2	V2	V2	V2	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V1
V2C-T	V-dump	V1	V1	V1	V1	V1	V1	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V2
V3C-T	V-dump	V3	V3	V3	V3	V3	V3	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3
VSW8-U	V-dump	V-OFF	V3	V3	V3	V3	V3	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3
V1D-T	V-dump	V-dump	V2	V2	V2	V2	V2	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V1
V2D-T	V-dump	V-dump	V1	V1	V1	V1	V1	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V2
V3D-T	V-dump	V-dump	V3	V3	V3	V3	V3	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3
VSW16-U	V-dump	V-dump	V-OFF	V3	V3	V3	V3	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3
V1E-T	V-dump	V-dump	V-dump	V2	V2	V2	V2	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V1
V2E-T	V-dump	V-dump	V-dump	V1	V1	V1	V1	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V2
V3E-T	V-dump	V-dump	V-dump	V3	V3	V3	V3	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3
VSW32-U	V-dump	V-dump	V-dump	V-OFF	V3	V3	V3	V-dump	V-dump	V-dump	V-dump	V-dump	V-OFF	V3
V1F-T	V-dump	V-dump	V-dump	V-dump	V2	V2	V2	V-dump	V-dump	V-dump	V-dump	V-dump	V1	V1

Pin Connection Table for each TDI mode

Pin Name	TDI-4 UP	TDI-8 UP	TDI-16 UP	TDI-32 UP	TDI-64 UP	TDI-96 UP	TDI-128 UP	TDI-4 DOWN	TDI-8 DOWN	TDI-16 DOWN	TDI-32 DOWN	TDI-64 DOWN	TDI-96 DOWN	TDI-128 DOWN
V2F-T	V-dump	V-dump	V-dump	V-dump	V1	V1	V1	V-dump	V-dump	V-dump	V-dump	V-dump	V2	V2
V3F-T	V-dump	V-dump	V-dump	V-dump	V3	V3	V3	V-dump	V-dump	V-dump	V-dump	V-dump	V3	V3
VSW64	V-dump	V-dump	V-dump	V-dump	V-OFF	V3	V3	V-dump	V-dump	V-dump	V-dump	V-OFF	V3	V3
V1F-B	V-dump	V-dump	V-dump	V-dump	V-dump	V2	V2	V-dump	V-dump	V-dump	V-dump	V1	V1	V1
V2F-B	V-dump	V-dump	V-dump	V-dump	V-dump	V1	V1	V-dump	V-dump	V-dump	V-dump	V2	V2	V2
V3F-B	V-dump	V-dump	V-dump	V-dump	V-dump	V3	V3	V-dump	V-dump	V-dump	V-dump	V3	V3	V3
VSW32-D	V-dump	V-dump	V-dump	V-dump	V-dump	V-OFF	V3	V-dump	V-dump	V-dump	V-OFF	V3	V3	V3
V1E-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V2	V-dump	V-dump	V-dump	V1	V1	V1	V1
V2E-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V1	V-dump	V-dump	V-dump	V2	V2	V2	V2
V3E-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3	V-dump	V-dump	V-dump	V3	V3	V3	V3
VSW16-D	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3	V-dump	V-dump	V-OFF	V3	V3	V3	V3
V1D-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V2	V-dump	V-dump	V1	V1	V1	V1	V1
V2D-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V1	V-dump	V-dump	V2	V2	V2	V2	V2
V3D-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3	V-dump	V-dump	V3	V3	V3	V3	V3
VSW8-D	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3	V-dump	V-OFF	V3	V3	V3	V3	V3
V1C-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V2	V-dump	V1	V1	V1	V1	V1	V1
V2C-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V1	V-dump	V2	V2	V2	V2	V2	V2
V3C-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3	V-dump	V3	V3	V3	V3	V3	V3
VSW4-D	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3	V-OFF	V3	V3	V3	V3	V3	V3
V1A-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V2	V1	V1	V1	V1	V1	V1	V1
V2A-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V1	V2	V2	V2	V2	V2	V2	V2
V3A-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3	V3	V3	V3	V3	V3	V3	V3
VSW128-U	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-OFF	V3	V3	V3	V3	V3	V3	V3
V1X-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V1	V1	V1	V1	V1	V1	V1
V2X-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V2	V2	V2	V2	V2	V2	V2
V3X-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V3	V3	V3	V3	V3	V3	V3
V1HS-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	VHS1	VHS1	VHS1	VHS1	VHS1	VHS1	VHS1
V2HS-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	VHS2	VHS2	VHS2	VHS2	VHS2	VHS2	VHS2
V3HS-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	VHS3	VHS3	VHS3	VHS3	VHS3	VHS3	VHS3
VTG-B	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	V-dump	VHS3	VHS3	VHS3	VHS3	VHS3	VHS3	VHS3
H1-Bx	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump	H1	H1	H1	H1	H1	H1	H1
H2-Bx	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump	H2	H2	H2	H2	H2	H2	H2
H3-Bx	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump	H3	H3	H3	H3	H3	H3	H3
H4-Bx	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump	H-dump	H4	H4	H4	H4	H4	H4	H4
FOG-Bx	(note 2)	(note 2)	(note 2)	(note 2)	(note 2)	(note 2)	(note 2)	ϕOG	ϕOG	ϕOG	ϕOG	ϕOG	ϕOG	ϕOG
RG-Bx	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	ϕR	ϕR	ϕR	ϕR	ϕR	ϕR	ϕR

Pin Connection Table for each TDI mode														
Pin Name	**TDI-4 UP**	**TDI-8 UP**	**TDI-16 UP**	**TDI-32 UP**	**TDI-64 UP**	**TDI-96 UP**	**TDI-128 UP**	**TDI-4 DOWN**	**TDI-8 DOWN**	**TDI-16 DOWN**	**TDI-32 DOWN**	**TDI-64 DOWN**	**TDI-96 DOWN**	**TDI-128 DOWN**
VDD-Bx	(note 4)	(note 4)	(note 4)	(note 4)	(note 4)	(note 4)	(note 4)	VDD	VDD	VDD	VDD	VDD	VDD	VDD
VSRC-Bx	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC	VSRC
VGT-Bx	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT
VRD-Bx	VRD	VRD	VRD	VRD	VRD	VRD	VRD	VRD	VRD	VRD	VRD	VRD	VRD	VRD
VOFD-Bx	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD	VOFD

Note 1: Connect to H-dump, or hold at RG (ϕR) clock-high, or clock with RG (ϕR).

Note 2: Connect to H-dump, or hold at FOG (ϕOG) clock-high, or clock with FOG (ϕOG).

Note 3: x={1,2,..8} for CCD5061; {1,2,…6} for CCD5061, (1,2,…4} for CCD5061.

Note 4: VDD connections on dump side: If the CCD5061 (or CCD5061 or CCD5061) always transfers only in one direction (either up or down), then to minimize power dissipation (a) connect dump side VDD pins to VSRC, and (b) do not install dump side R_{LOAD} resistors. If the CCD5061/CCD5061/CCD5061 is used alternately up and down, then connect "dump" side VDD pins to VDD to avoid power-up / power-down R*C time constant problems, or power down dump side VDD to approximately +10VDC.

Pinout Diagram

	A	B	C		D	E	F	
1	VSS	TEMP T1 +	TEMP T1 -		VSS	VSS	VSS	**1**
2	F2-T	F3-T	VSW64		F3-B	F2-B	F1-B	**2**
3	E3-T	VSW32U	F1-T		VSW32D	E3-B	E2-B	**3**
4	VSW16U	E1-T	E2-T		VSS	E1-B	VSW16D	**4**
5	D1-T	D2-T	D3-T		D3-B	D2-B	D1-B	**5**
6	C2-T	C3-T	VSW8U		VSW8D	C3-B	C2-B	**6**
7	AB3-T	VSW4U	C1-T		C1-B	VSW4D	AB3-B	**7**
8	VSW128D	AB1-T	AB2-T		AB2-B	AB1-B	VSW128U	**8**
9	X1-T	X2-T	X3-T		X3-B	X2-B	X1-B	**9**
10	NC	VGT-T	VOFD-T		VOFD-B	VGT-B	NC	**10**
11	NC	NC	NC		NC	NC	NC	**11**
12	NC	NC	NC		NC	NC	NC	**12**
13	NC	NC	NC		NC	NC	NC	**13**
14	VSRC-T1	NC	NC		NC	NC	VSRC-B1	**14**
15	VDD-T1	VSS	VOUT-T1		VOUT-B1	VSS	VDD-B1	**15**
16	VOG-T1	ϕR-T1	VRD-T1		VRD-B1	ϕR -B1	VOG-B1	**16**
17	H2-T1	ϕOG-T1	H3-T1		H3-B1	ϕOG-B1	H2-B1	**17**
18	VSRC-T2	H1-T1	H4-T1		H4-B1	H1-B1	VSRC-B2	**18**
19	VDD-T2	VSS	VOUT-T2		VOUT-B2	VSS	VDD-B2	**19**
20	VOG-T2	ϕR -T2	VRD-T2		VRD-B2	ϕR -B2	VOG-B2	**20**
21	H2-T2	ϕOG-T2	H3-T2		H3-B2	ϕOG-B2	H2-B2	**21**
22	VSRC-T3	H1-T2	H4-T2		H4-B2	H1-B2	VSRC-B3	**22**
23	VDD-T3	VSS	VOUT-T3		VOUT-B3	VSS	VDD-B3	**23**
24	VOG-T3	ϕR -T3	VRD-T3		VRD-B3	ϕR -B3	VOG-B3	**24**
25	H2-T3	ϕOG-T3	H3-T3		H3-B3	ϕOG-B3	H2-B3	**25**
26	VSRC-T4	H1-T3	H4-T3		H4-B3	H1-B3	VSRC-B4	**26**
27	VDD-T4	VSS	VOUT-T4		VOUT-B4	VSS	VDD-B4	**27**
28	ϕR -T4	VOG-T4	VRD-T4		VRD-B4	VOG-B4	ϕR -B4	**28**
29	ϕOG-T4	H2-T4	H4-T4		H4-B4	H2-B4	ϕOG-B4	**29**
30	NC	H3-T4	H1-T4		H1-B4	H3-B4	NC	**30**
31	NC	NC	NC		NC	NC	NC	**31**
32	NC	NC	NC		NC	NC	NC	**32**
33	NC	NC	NC		NC	NC	NC	**33**
34	VTG-T	NC	NC		NC	NC	VTG-B	**34**
35	VHS3-T	VHS2-T	VHS1-T		VHS1-B	VHS2-B	VHS3-B	**35**
36	X1-T	X2-T	X3-T		X3-B	X2-B	X1-B	**36**
37	VSW128D	AB1-T	AB2-T		AB2-B	AB1-B	VSW128U	**37**
38	AB3-T	VSW4U	C1-T		C1-B	VSW4D	AB3-B	**38**
39	C2-T	C3-T	VSW8U		VSW8D	C3-B	C2-B	**39**
40	D1-T	D2-T	D3-T		D3-B	D2-B	D1-B	**40**
41	VSW16U	E1-T	VSS		E2-B	E1-B	VSW16D	**41**
42	E2-T	E3-T	VSW32U		F1-B	VSW32D	E3-B	**42**
43	F1-T	F2-T	F3-T		VSW64	F3-B	F2-B	**43**
44	VSS	VSS	VSS		TEMP B4 -	TEMP B4 +	VSS	**44**

Note: NC = Not connected

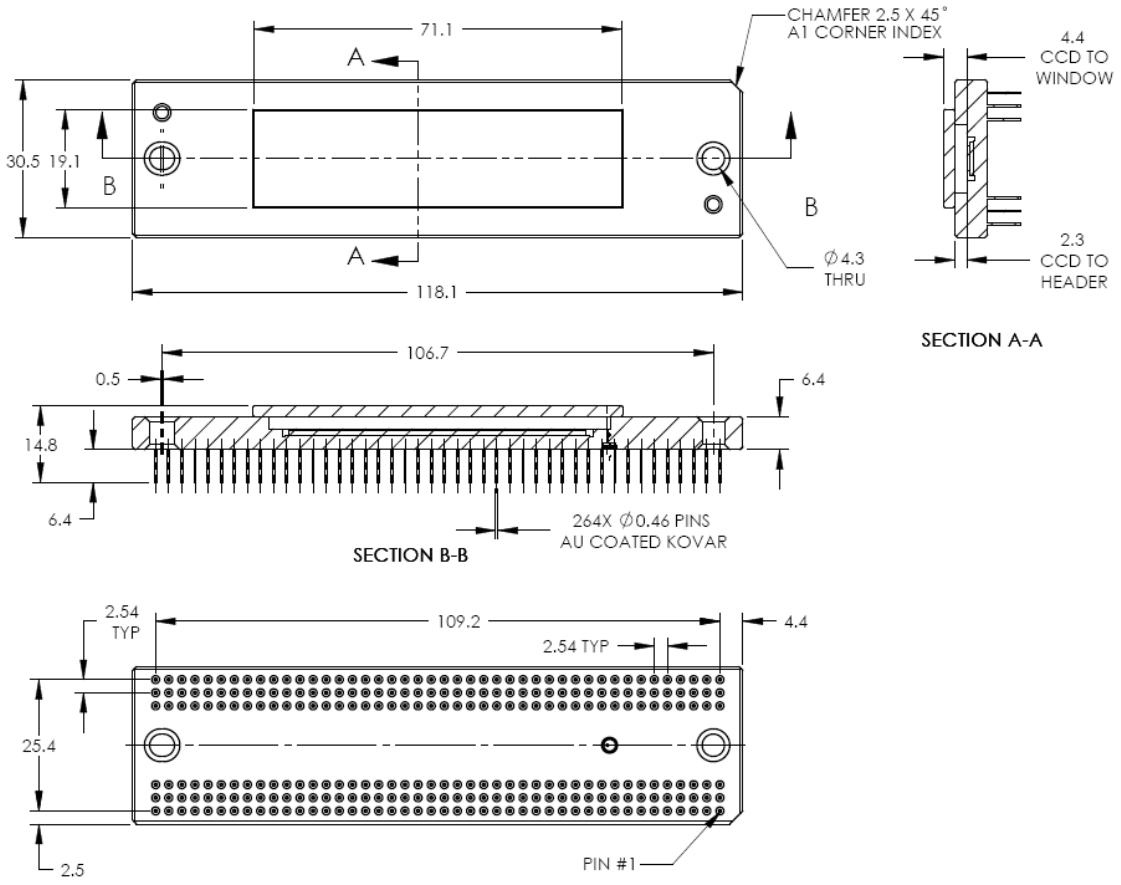
CCD HANDLING PRECAUTIONS TO PREVENT ESD DAMAGE

By their very nature, CCDs are very sensitive to electro-static discharge (ESD) damage. Special ESD-control equipment and personnel training are mandatory, particularly when installing or removing the CCD from a camera system. See Fairchild Imaging application note “Prevention of ESD Damage in CCD Image Sensors” for details. Key points:

- Use ESD-safe workbench surfaces. Cover metallic workbench surfaces with ESD-safe grounded mats. Remove non-ESD-safe materials (paper, tools with plastic handles, etc.) from work area.
- Use wrist straps or equivalent (~1MΩ to ground), ESD-safe lab coat or equivalent (buttoned—not open), and ESD-safe gloves or finger cots. Test wrist strap before handling CCDs.
- Relative humidity must be 40% min.; >50% recommended.
- Use ionizing air blowers; type: AC (not pulsed DC), balance $\leq |\pm 20V|$ max., $\leq |\pm 10V|$ recommended. Performance spec at work area: voltage decay from 1000V to 100V in <10 seconds. Measure this periodically; air ionizers require maintenance.
- Allow devices to slowly discharge in the ionized air stream when removing devices from their 1st-level container, and when removing devices from test sockets.
- The receiving socket and associated circuitry must be adequately grounded.
- Store CCDs with all pins shorted together by shorting bars, conductive foam, or the equivalent.

ESD damage invalidates the warranty.

Package Diagram



Drawing Notes:

1. Dimensions in mm
2. Die flatness refer to F_{PIXEL} in Performance Specifications on page 8.

COSMETIC GRADING

Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels and at different operating temperatures.

WARRANTY

Fairchild Imaging warrants that its products will be free of defects in material and workmanship under normal use and service for one year from date of shipment

CERTIFICATION

Fairchild Imaging certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specifications under which it is furnished.

This product is designed, manufactured and distributed utilizing the ISO 9000:2000 Business Management System.